(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 394 722 A3**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 90106557.3

(51) Int. Cl.5 H01L 21/90, H01L 23/532

(22) Date of filing: 05.04.90

(30) Priority: 05.04.89 JP 87513/89

(43) Date of publication of application:
31.10.90 Bulletin 90/44

(84) Designated Contracting States:
DE FR GB

(88) Date of deferred publication of the search report:
08.01.92 Bulletin 92/02

(71) Applicant: NEC CORPORATION
7-1, Shiba 5-chome Minato-ku
Tokyo 108-01(JP)

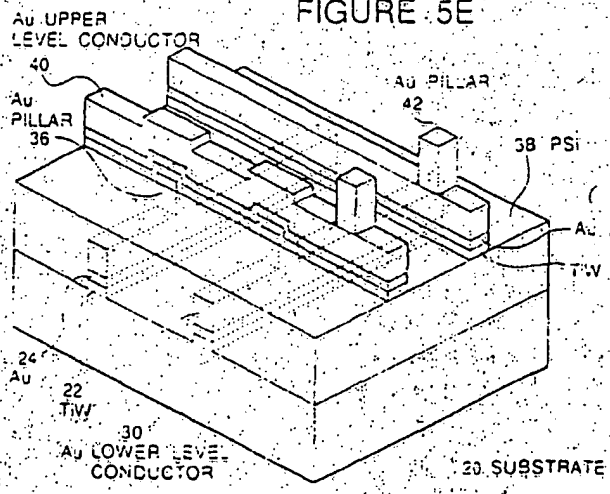
(72) Inventor: Kudoh, Osamu
c/o NEC Corporation, 7-1, Shiba 5-chome
Minato-ku, Tokyo 108-01(JP)
Inventor: Okada, Kenji
c/o NEC Corporation, 7-1, Shiba 5-chome
Minato-ku, Tokyo 108-01(JP)
Inventor: Shiba, Hiroshi
c/o NEC Corporation, 7-1, Shiba 5-chome
Minato-ku, Tokyo 108-01(JP)

(74) Representative: Glawe, Delfs, Moll & Partner
Patentanwälte
Postfach 26 01 62 Liebherrstrasse 20
W-8000 München 26(DE)

(54) Multilevel metallization for VLSI and method for forming the same.

(57) An integrated circuit includes a substrate, a first level horizontal conductor formed on the substrate, an interlayer insulator formed to cover the first level conductor, a second level horizontal conductor formed on the interlayer insulator, and a vertical conductive pillar extending through the interlayer insulator for interconnecting the first level horizontal conductor and the second level horizontal conductor. The vertical conductive pillar has a side surface coplanar with a longitudinal side surface of the first level horizontal conductor at a position where the vertical conductive pillar is in electric contact with the first level horizontal conductor.

FIGURE 5E



EP 0 394 722 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 10 6557

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP-A-0 129 389 (PLESSEY OVERSEAS LIMITED)	1	H 01 L 21 90 H 01 L 23 532
A	EP-A-0 129 389 (-) figure 5	2.8	
A,D	IEEE VLSI MULTILEVEL INTERCONNECT CONF. 1988. 13-14 6/88. p 117-124. K. HABERLE ET AL. "MULTILEVEL GOLD METALLISATION"	3.4.8	
A	the whole document	3.4.8	
A	US-A-4 614 021 (HULSEWEH)	6,7	
A	US-A-4 614 021 (" abstract ")	6.7	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	06 November 91	PHEASANT N.J.

CATEGORY OF CITED DOCUMENTS

- X: particularly relevant if taken alone
- Y: particularly relevant if combined with another document of the same catagory
- A: technological background
- O: non-written disclosure
- P: intermediate document
- T: theory or principle underlying the invention
- E: earlier patent document, but published on, or after the filing date
- D: document cited in the application
- L: document cited for other reasons
- &: member of the same patent family, corresponding document

FIGURE 5E

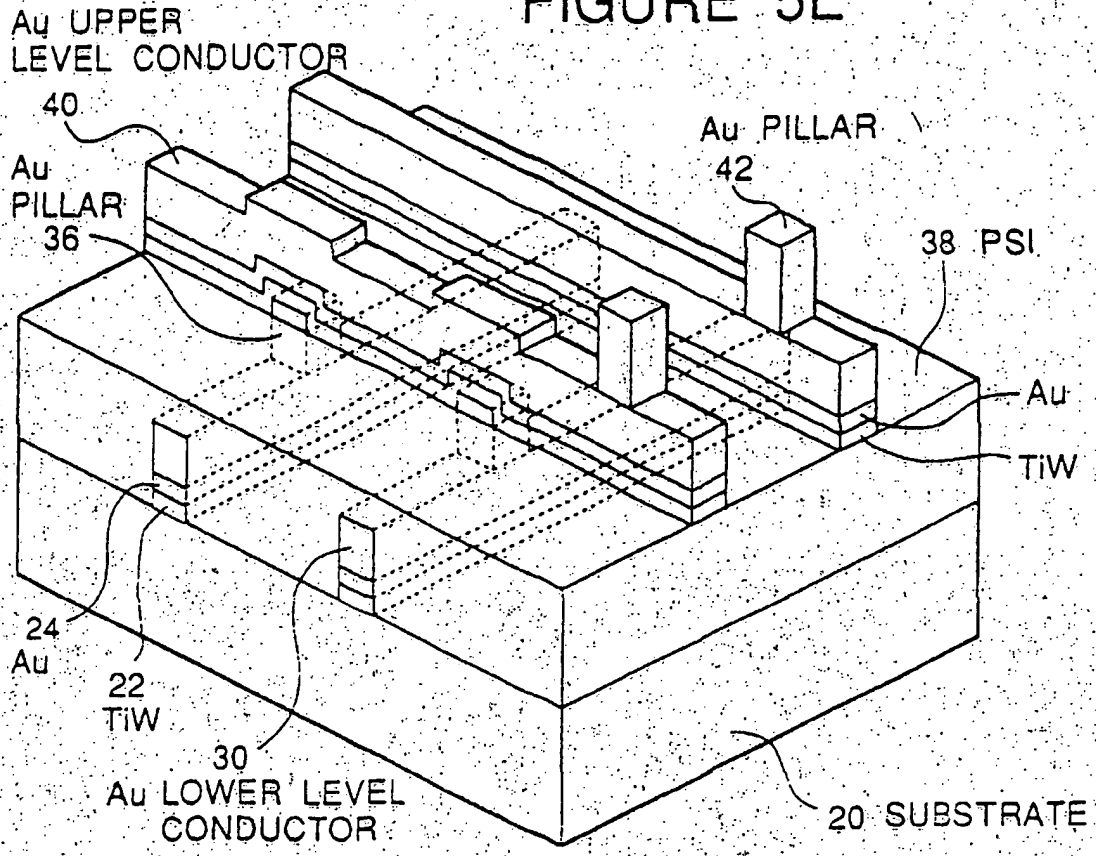


FIGURE 6

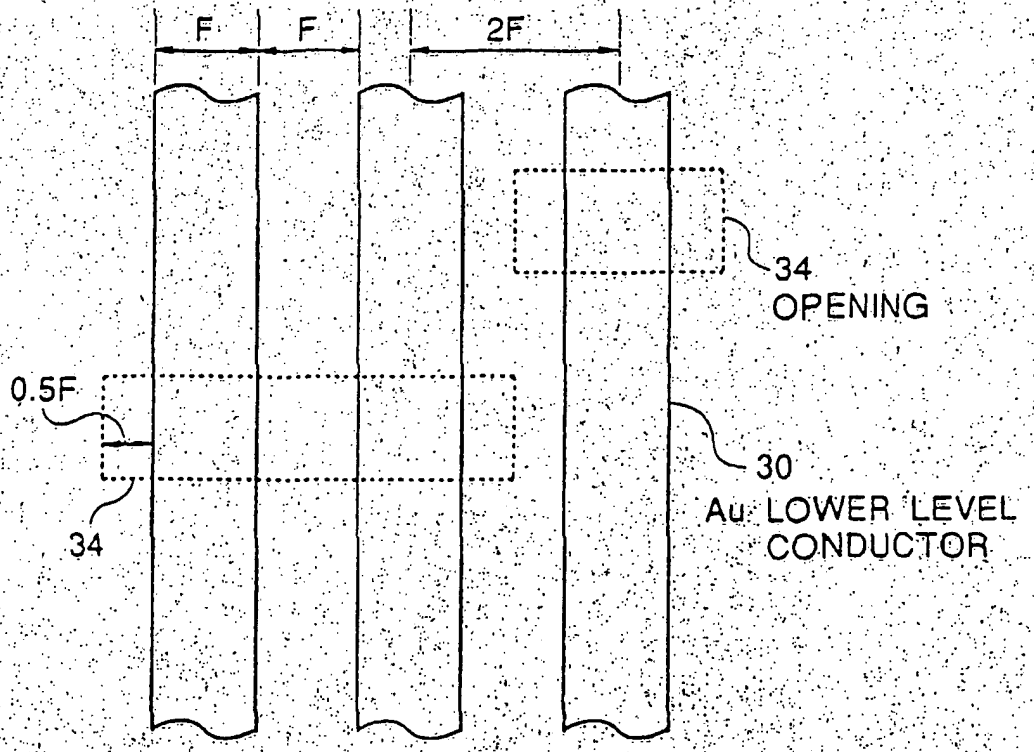


FIGURE 5C

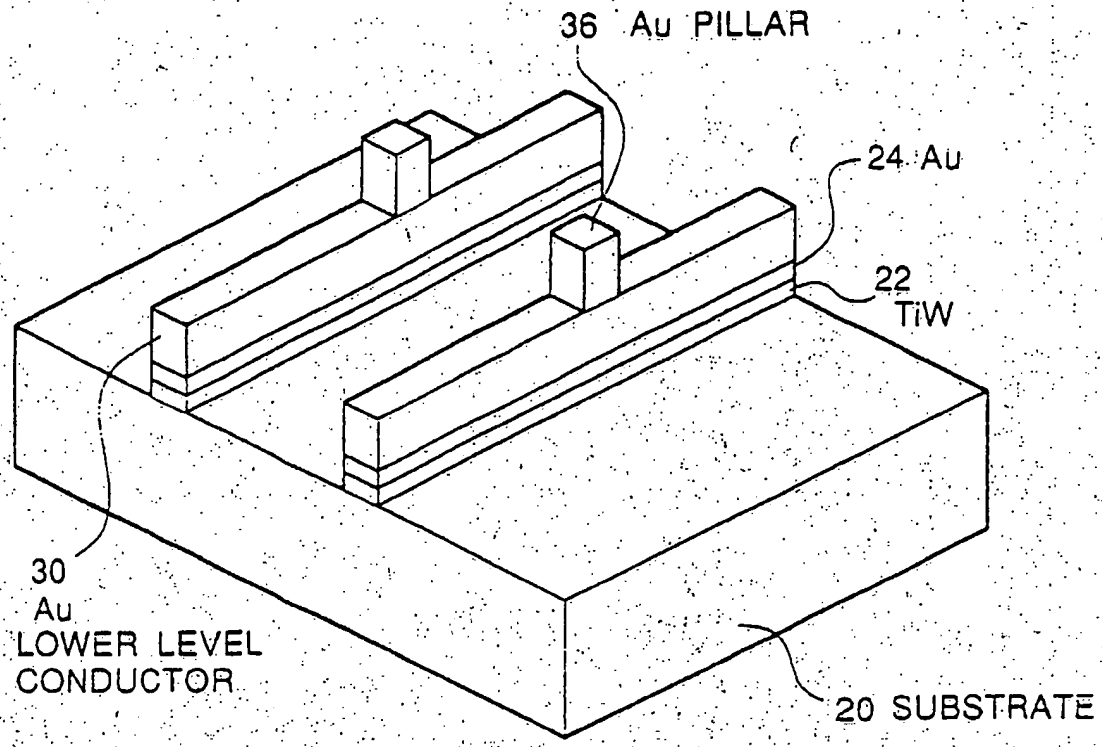


FIGURE 5D

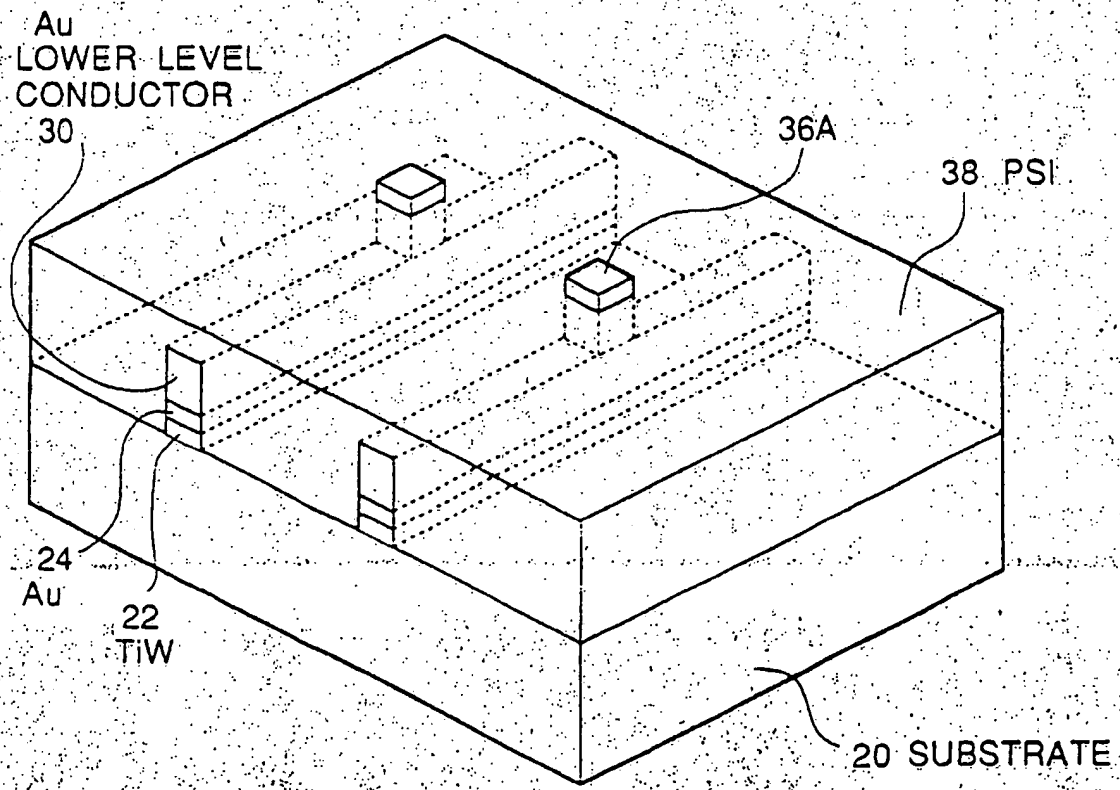


FIGURE 5A

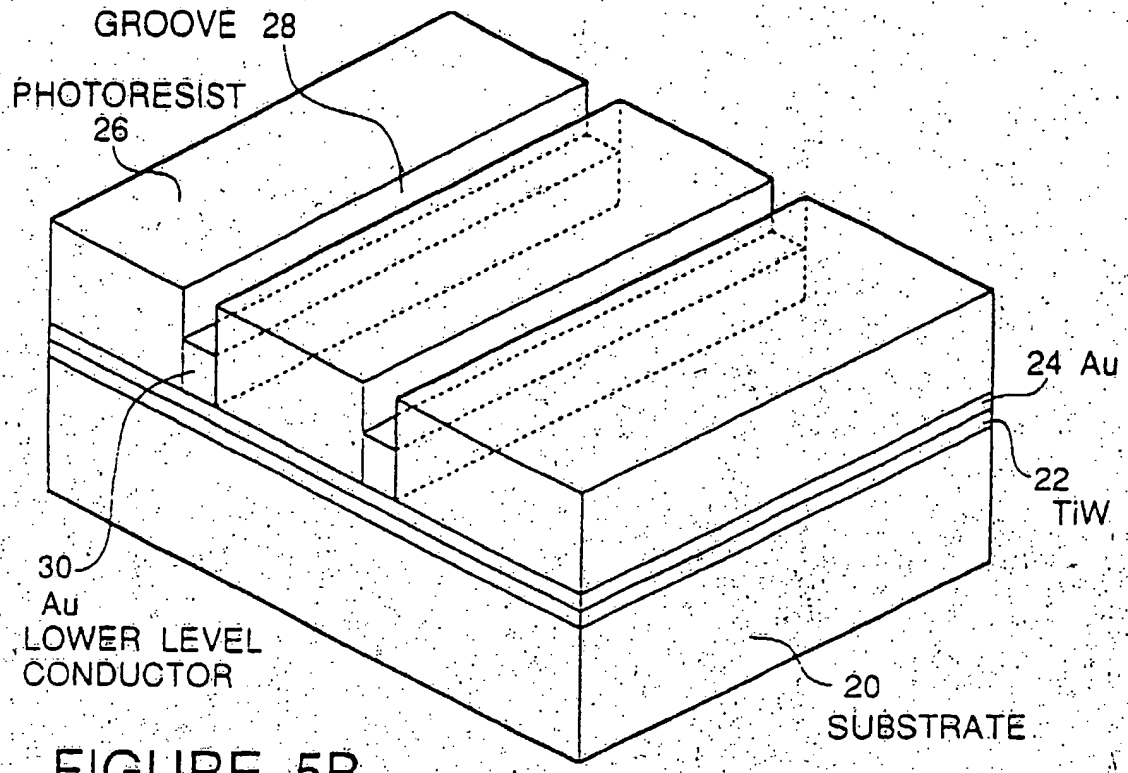


FIGURE 5B

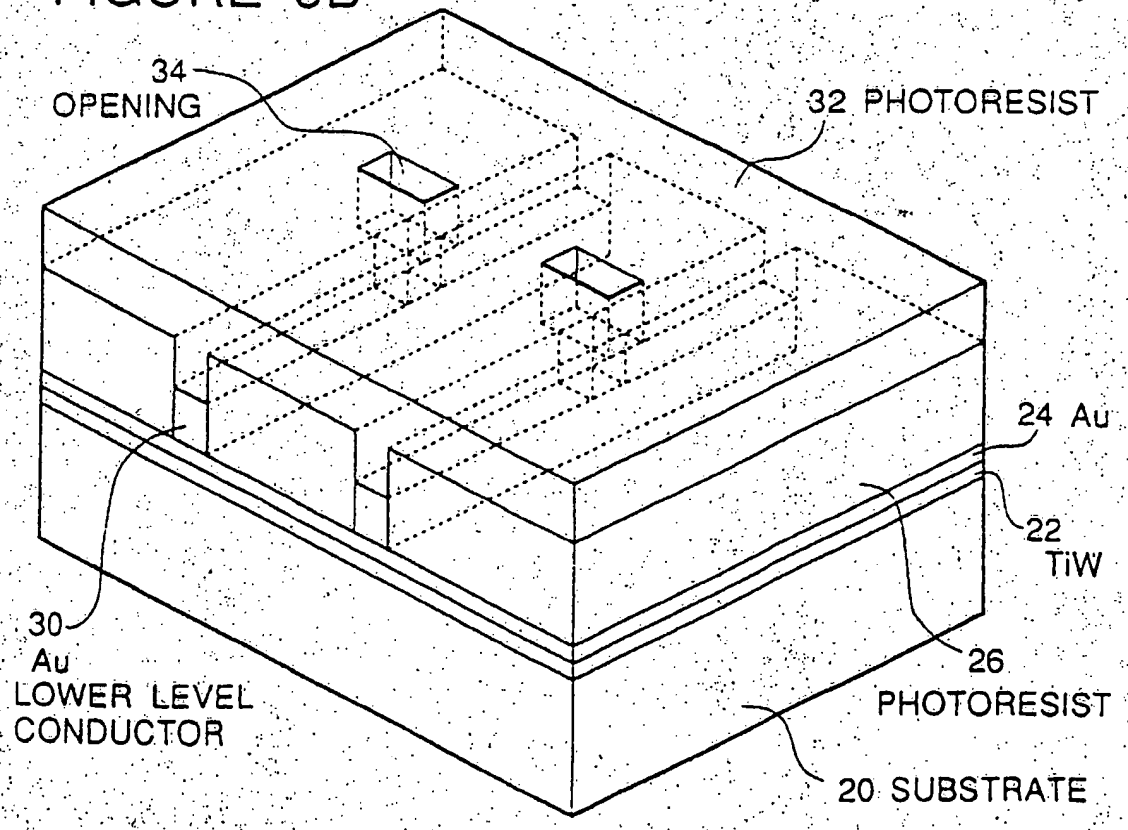


FIGURE 3
PRIOR ART

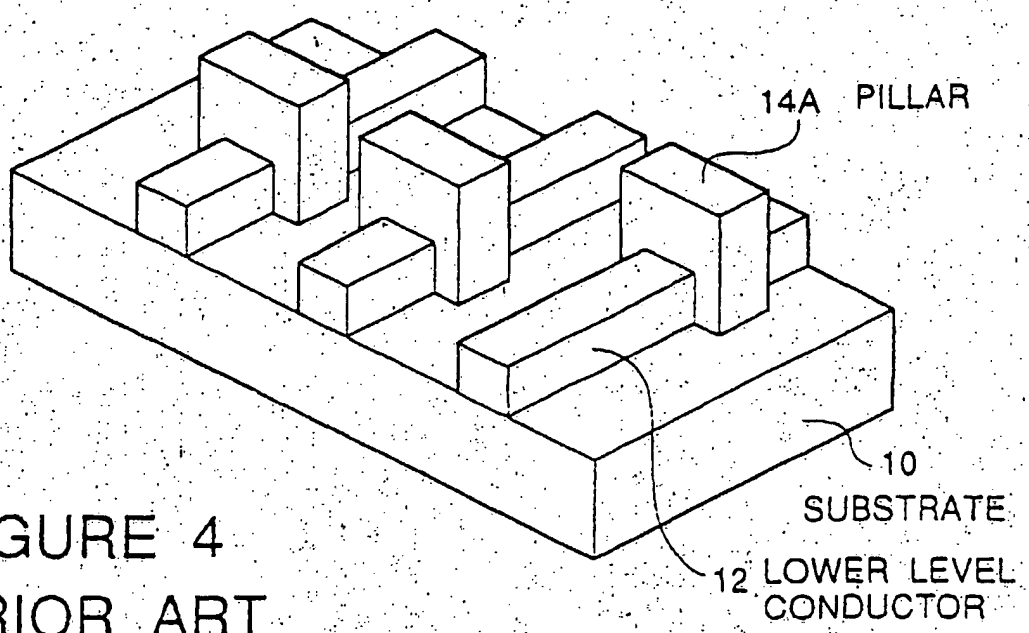


FIGURE 4
PRIOR ART

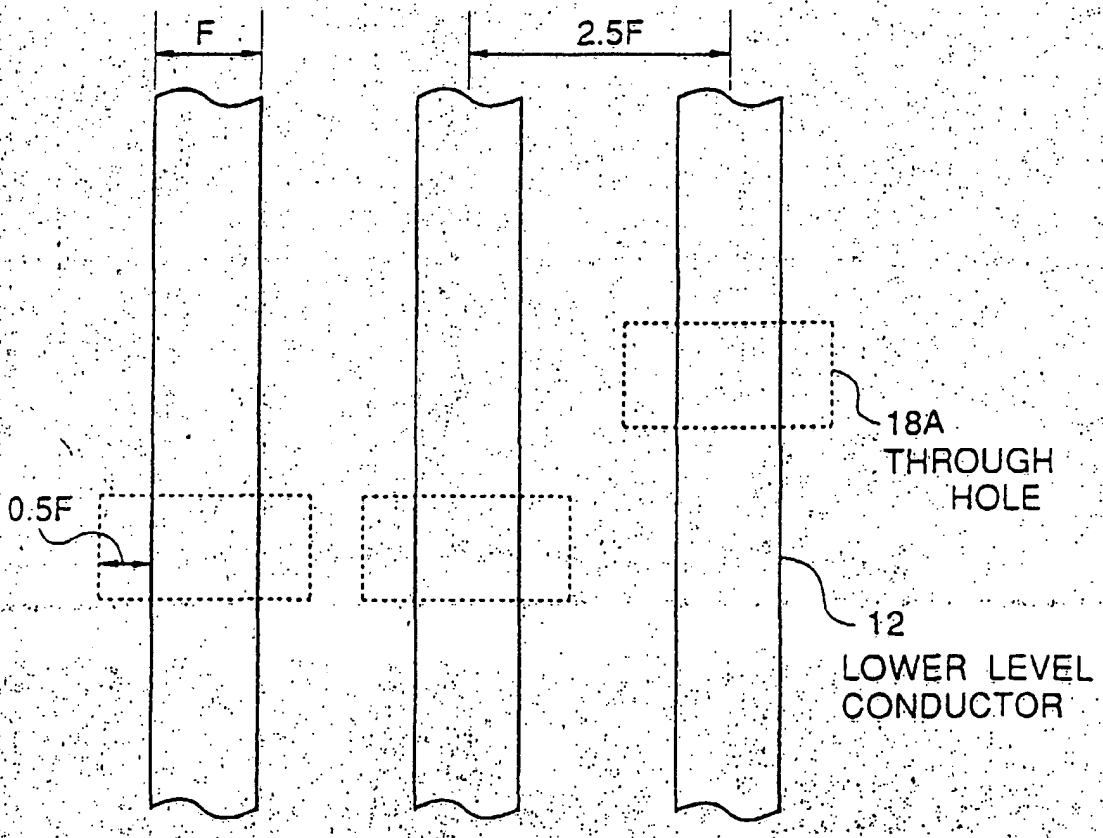


FIGURE 1
PRIOR ART

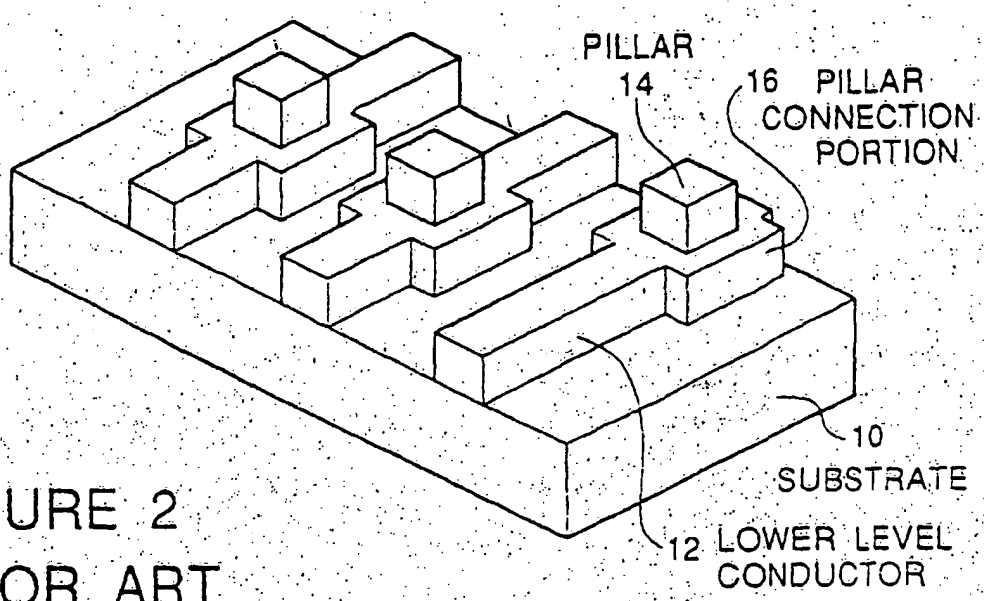
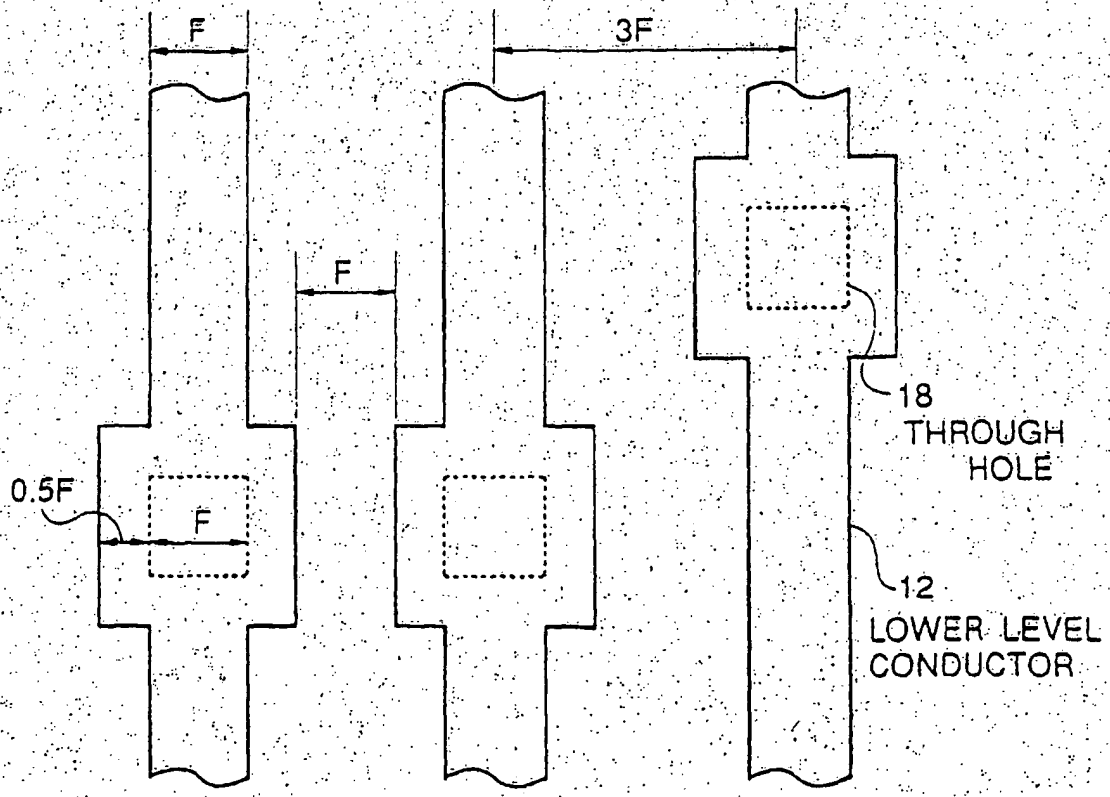


FIGURE 2
PRIOR ART



the first and second photoresists.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 394 722**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 90106557.3

(51) Int. Cl.5: H01L 21/90, H01L 23/532

(22) Date of filing: 05.04.90

(30) Priority: 05.04.89 JP 87513/89

(43) Date of publication of application: 31.10.90 Bulletin 90/44

(84) Designated Contracting States: DE FR GB

(71) Applicant: NEC CORPORATION
7-1, Shiba 5-chome Minato-ku
Tokyo 108-01(JP)

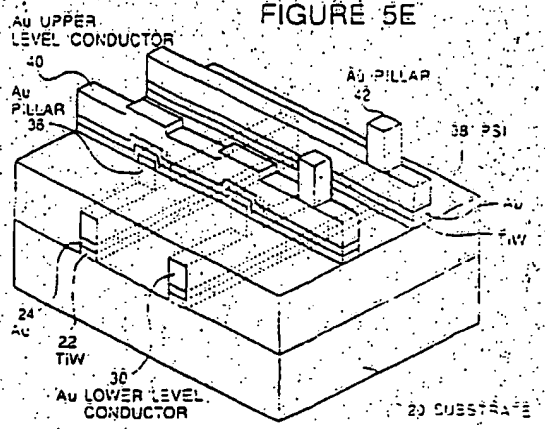
(72) Inventor: Kudoh, Osamu
c/o NEC Corporation, 7-1, Shiba 5-chome
Minato-ku, Tokyo 108-01(JP)
Inventor: Okada, Kenji
c/o NEC Corporation, 7-1, Shiba 5-chome
Minato-ku, Tokyo 108-01(JP)
Inventor: Shiba, Hiroshi
c/o NEC Corporation, 7-1, Shiba 5-chome
Minato-ku, Tokyo 108-01(JP)

(74) Representative: Glawe, Delfs, Moll & Partner
Patentanwälte
Postfach 26 01 62 Liebherrstrasse 20
D-8000 München 26(DE)

(54) Multilevel metallization for VLSI and method for forming the same.

(57) An integrated circuit includes a substrate, a first level horizontal conductor formed on the substrate, an interlayer insulator formed to cover the first level conductor, a second level horizontal conductor formed on the interlayer insulator, and a vertical conductive pillar extending through the interlayer insulator for interconnecting the first level horizontal conductor and the second level horizontal conductor. The vertical conductive pillar has a side surface coplanar with a longitudinal side surface of the first level horizontal conductor at a position where the vertical conductive pillar is in electric contact with the first level horizontal conductor.

FIGURE 5E



EP 0 394 722 A2

MULTILEVEL METALLIZATION FOR VLSI AND METHOD FOR FORMING THE SAME

Background of the Invention

Field of the invention

The present invention relates to a multilevel metallization and a method for forming the same, and more specifically to an improved pillar structure for interconnection between two different levels of wiring conductors, and a method for forming the improved pillar connection.

Description of related art

In the prior art, a vertical connection between two different levels of wiring conductors in a multilevel metallization has been effected by completely charging a conducting material into a through hole or via hole formed in an interlayer insulating layer, by vacuum evaporation or by sputtering. However, an advanced integrated circuit technology, particularly, an increased integration density of the integrated circuit has made it difficult to realize a stable interlayer interconnection by means of through holes. In order to overcome this problem, it has been proposed to previously form a stud-like connection member, often called a "pillar", on a lower level metallization so as to vertically protrude from the lower level metallization, whereby a good interlayer connection between the lower level metallization and an upper level metallization can be realized by the conductive pillar vertically protruding from the lower level metallization.

Referring to Figures 1 and 2, there are diagrammatically shown a typical example of a conventional conductive pillar vertically protruding from the lower level metallization. As shown in Figure 1, a plurality of lower level conductors 10 are formed on a semiconductor substrate 12, and a conductive pillar 14 is formed on the lower level conductor 10 at a portion 16 where a through hole 18 is to be formed in an interlayer insulator (not shown) which is to be formed to cover the lower level conductors 10 for the purpose of interconnection between the lower level conductors 10 and an upper level conductor (not shown) to be formed on the interlayer insulator. As seen from Figure 2, however, in order to previously ensure a tolerance of alignment and to compensate for variation of dimensional accuracy in the semiconductor process, it has been necessary to widen the portion 16 of the lower level conductor 12 where the pillar 14 is formed, with the result that a conductor pattern pitch (line pitch) must be enlarged. For example, assuming that a width of each conductor 12 is "F" at a portion excluding the pillar formation portion 16 and "2F" at the pillar formation portion 16, and that a minimum space between each pair of adjacent conductors is "F", the conductor pattern pitch must be "3F". In other words, it is disadvantageous that the wiring density has been decreased.

Recently, K. Haberle et al proposed in Proceedings of IEEE V-MIC Conference, 1988, pp117-124, that the wiring conductors and the pillars are formed of gold metallization so as to reduce the wiring pitch. Referring to Figures 3 and 4, there are diagrammatically shown a conductive pillar proposed by K. Haberle et al. As shown in Figure 4, a through hole 18A is formed to have a size larger than the width of the lower level conductor 12 formed on the substrate 10, and then, as shown in Figure 3, a pillar 14A is formed to straddle the lower level conductor 12 by means of a gold plating method.

In this method, assuming that the width of each lower level conductor 12 is "F" and the width of the pillar 14A is "2F", in a direction perpendicular to the longitudinal direction of the lower level conductor 12, the wiring pitch (line pitch) can be made "2.5F", which is shorter than the example shown in Figures 1 and 2. However, due to possible misalignment of mask patterns and due to variations of the shape of the pillar, there is an danger of short-circuiting between adjacent conductors or another danger of increasing a wiring capacitance even if the adjacent conductors are not short-circuited. In other words, in order to avoid these dangers, the wiring pitch (line pitch) cannot be sufficiently reduced.

Summary of the Invention

Accordingly, it is an object of the present invention to provide an interlayer connection structure for an integrated circuit, which has overcome the above mentioned defect of the conventional one.

Another object of the present invention is to provide an interlayer connection structure of the pillar type, which can reduce the wiring pitch as compared with the conventional one.

Still another object of the present invention is to provide a method of forming an interlayer connection structure of the pillar type, which allows to reduce the wiring pitch as compared with the conventional methods.

The above and other objects of the present

invention are achieved in accordance with the present invention by an integrated circuit including a substrate, a first level horizontal conductor formed on the substrate, an interlayer insulator formed to cover the first level conductor, a second level horizontal conductor formed on the interlayer insulator, and a conductive pillar extending through the interlayer insulator for interconnecting the first level horizontal conductor and the second level horizontal conductor, the conductive pillar having a pair of opposite side surfaces coplanar with a pair of corresponding longitudinal side surfaces of the first level horizontal conductor at a position where the conductive pillar is in electric contact with the first level horizontal conductor.

According to another aspect of the present invention, there is provided a method of forming an interlayer connection conductor in an integrated circuit, comprising the steps of depositing a first photoresist layer on the conducting layer and patterning the deposited first photoresist layer to form in the deposited first photoresist layer a groove for formation of a lower level wiring conductor, forming within the groove a first level wiring conductor having a thickness smaller than that of the deposited first photoresist layer, forming a second photoresist to cover an area including the first level wiring conductor, forming an opening in the second photoresist above the lower level wiring conductor at a predetermined position where the lower level wiring conductor is to be interconnected with a possible upper level wiring conductor, so that a portion of the lower level wiring conductor is exposed through the opening, the opening having a size larger than a width of the lower level wiring conductor, and forming a conductive pillar within the opening, so that the conductive pillar is formed in the groove above the lower level wiring conductor.

As seen from the above, the interlayer connection structure in accordance with the present invention for an integrated circuit is such that a pair of opposite side surfaces of the conductive pillar vertically extruding from the first level horizontal conductor are coplanar with a pair of corresponding longitudinal side surfaces of the first level horizontal conductor, respectively. This means that the dimension of the conductive pillar in a width direction of the first level horizontal conductor has the same as the width of the first level horizontal conductor, and accordingly, the wiring pitch can be determined by the width of the first level horizontal conductor and therefore can be reduced as compared with the conventional one.

In addition, in the method in accordance with the present invention for forming the interlayer connection structure, the lower level wiring conductor and the conductive pillar are formed within the groove formed in the deposited first photoresist layer. This means that the conductive pillar is formed in a self-alignment with the lower level wiring conductor by action of the groove formed in the deposited first photoresist layer. Therefore, the wiring pitch can be reduced to a limit determined by a photolithography. In other words, the wiring pitch can become free from a tolerance margin for misalignment and a dimensional error of semiconductor process, which were causes for increasing the wiring pitch in the prior art.

The above and other objects, features and advantages of the present invention will be apparent from the following description of a preferred embodiment of the invention with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a diagrammatic perspective view of one example of the conventional conductive pillar vertically protruding from the lower level conductor in the multilevel metallization;

Figure 2 is a wiring pattern diagram of the lower level conductor and the conductive pillar vertically protruding therefrom as shown in Figure 1;

Figure 3 is a diagrammatic perspective view of another example of the conventional conductive pillar vertically protruding from the lower level conductor in the multilevel metallization;

Figure 4 is a wiring pattern diagram of the lower level conductor and the conductive pillar vertically protruding therefrom as shown in Figure 3;

Figure 5A to 5E are diagrammatic perspective views of an integrated circuit chip for illustrating one embodiment of the pillar type interlayer connection construction forming method in accordance with the present invention; and

Figure 6 is a wiring pattern diagram of the lower level conductor and the conductive pillar vertically protruding therefrom formed in the method illustrated in Figures 5A to 5E.

Description of the Preferred embodiment

Referring to Figure 5A to 5E, there are shown diagrammatic perspective views of an integrated circuit chip for illustrating one embodiment of the pillar type interlayer connection construction forming method in accordance with the presnt invention.

Firstly, in order to form a conductive underlayer which is used for forming necessary wiring conductors and vertical conductive pillars on a semiconductor substrate 20 by use of an Au (gold) electroplating method, a thin layer 22 of TiW and another thin layer 24 of Au are continuously depos-

ited on a principal surface of the semiconductor substrate 20 by sputtering. Thereafter, a first photoresist 26 is deposited to cover the whole of the principal surface of the semiconductor substrate 20 and to have a thickness of 2.0μm, and the deposited first photoresist is patterned by a photolithography to form a plurality of grooves 28 for a lower level conductor, so that the underlying Au thin layer 24 is exposed within the grooves 28. Then, as shown in Figure 5A, a first or lower level conductor 30 of Au having a thickness of 0.8μm is formed within each groove 28, namely deposited on the exposed underlying Au thin layer 24 within each groove 28, by means of the Au electroplating method using the conducting underlayer 24 as an electrode to be plated. This Au electroplating method is described in detail in the K. Haberle et al article referred to hereinbefore, and therefore, a detailed explanation thereof will be omitted.

As shown in Figure 5B, a second photoresist 32 is deposited to cover the whole upper surface of the semiconductor substrate 20, with the portion of each groove 28 above the first or lower level conductor 30 being filled with the second photoresist 32. The deposited second photoresist 32 is patterned by a photolithography to form a plurality of openings 34, at predetermined positions where a conductive pillar is to be formed, so that the first or lower level conductor 30 is partially exposed. As shown in Figure 6, the size of the opening 34 in a direction perpendicular to a longitudinal direction of the first or lower level conductor 30 is larger than the width of the first or lower level conductor 30, namely, the width of the groove 28. Specifically, at a level above a horizontal boundary between the first photoresist 26 and the second photoresist 32, each opening 34 has the size larger than the width of the lower level conductor 30. On the other hand, at a level below the horizontal boundary between the first photoresist 26 and the second photoresist 32, each opening 34 has a size limited by the width of the groove 28, namely, the width of the lower level conductor 30. Accordingly, the relative positioning of the opening 34 to the first or lower level conductor 30 may be at a relatively low degree of accuracy, if there is assured that the full width of the lower level conductor 30 is exposed within the opening 34. In other words, a center of the opening is not necessarily in precise alignment to a longitudinal center axis of the lower level conductor 30.

Here, it should be noted that, for the photolithography for the second photoresist 32, it is necessary to select a process which gives no damage to the shape of the first photoresist 26. For example, if the first and second photoresists 26 and 32 is of a positive type which contains a Novorak resin as a main component, the first photoresist 26 is cured within a plasma atmosphere, and thereafter, the second photoresist 32 is deposited. With this, the second photoresist 32 can be patterned to a desired shape without giving a substantial damage to the shape of the first photoresist 26.

After the formation of the openings 34, Au is deposited by the Au electroplating method using the conducting underlayer 24 as an electrode to be plated, until a first pillar 36 of Au having a height of 0.8μm is grown on the lower level conductor 30 within the opening 34. The total height of the lower level conductor 30 and the first pillar 36 is 1.6μm, which is smaller than the thickness of the first photoresist 26. Therefore, a pair of opposite side surfaces of the first pillar 36 positioned in a longitudinal direction of the lower level conductor 30 are coplanar with a pair of corresponding opposite longitudinal side surfaces of the lower level conductor 30. In other words, although the opening 34 having the size larger than the width of the lower level conductor 30 is formed in the second photoresist 32, the first pillar 36 is formed in self-alignment with the lower level conductor 30.

Thereafter, the first and second photoresists 26 and 32 are removed, and then, the exposed underlayer composed of the Au layer 24 and TiW layer 22 is removed by means of ion milling, as shown in Figure 5C.

Then, as shown in Figure 5D, a silicone polyimide (PSI) layer 38 is deposited as an interlayer insulator on the whole surface of the substrate, and etched back by means of an entire etch-back process until a head portion 36A of the first pillar 36 is exposed above the silicone polyimide layer 38 so that the exposed portion has a height of 0.2μm.

Thereafter, as shown in Figure 5E, a required number of second or upper level conductors 40 and second pillars 42 of Au protruding from the upper level conductors 40 are formed in the same manner as that explained above with reference to Figures 5A to 5D. The upper level conductors 40 are formed in a direction orthogonal to the lower level conductors 30, and some of the upper level conductors 40 are formed above and in electric contact with selected ones of the exposed heads 36A of the first pillars 36. The second pillars 42 are formed in self alignment with the upper level conductors 40. Therefore, the upper level conductors 40 can be formed with the wiring pitch (line pitch) of 2F, similarly to the lower level conductors 30.

The process as mentioned above can be repeatedly performed. Therefore, a multilevel metallization can be realized with a desired number of levels and with a minimum wiring pitch (line pitch) allowed by the photolithography. Accordingly, an currently allowed maximum wiring density can be obtained.

The invention has thus been shown and described with reference to the specific embodiment. However, it should be noted that the present invention is in no way limited to the details of the illustrated structures but changes and modifications may be made within the scope of the appended claims.

Claims

1. An integrated circuit including a substrate, a first level horizontal conductor formed on the substrate, an interlayer insulator formed to cover the first level conductor, a second level horizontal conductor formed on the interlayer insulator, and a vertical conductive pillar extending through the interlayer insulator for interconnecting the first level horizontal conductor and the second level horizontal conductor, the vertical conductive pillar having a side surface coplanar with a longitudinal side surface of the first level horizontal conductor at a position where the vertical conductive pillar is in electric contact with the first level horizontal conductor.

2. An integrated circuit claimed in Claim 1 wherein the first level horizontal conductor extends in a first direction and has an upper surface and a pair of opposite longitudinal side surfaces which extending in the first direction, and the second level horizontal conductor extends in a second direction orthogonal to the first direction; the vertical conductive pillar being formed to extend from the upper surface of the first level horizontal conductor to a bottom surface of the second level horizontal conductor, the vertical conductive pillar having a pair of opposite side surfaces in parallel to and coplanar to the corresponding opposite longitudinal side surfaces of the first level horizontal conductor.

3. A method of forming an interlayer connection conductor in an integrated circuit, comprising the steps of depositing a first photoresist layer on the conducting layer and patterning the deposited first photoresist layer to form in the deposited first photoresist layer a groove for formation of a lower level wiring conductor, forming within the groove a first level wiring conductor having a thickness smaller than that of the deposited first photoresist layer, forming a second photoresist to cover an area including the first level wiring conductor, forming an opening in the second photoresist above the lower level wiring conductor at a predetermined position where the lower level wiring conductor is to be interconnected with a possible upper level wiring conductor, so that a portion of the lower level wiring conductor is exposed through the opening, the opening having a size larger than a width of the lower level wiring conductor, and forming a conductive pillar within the opening, so that the conductive pillar is formed in the groove above the lower level wiring conductor.

4. A method claimed in claim 3 wherein a conducting underlayer is formed on a principal surface of the substrate before depositing the first photoresist layer on the conducting layer, and wherein the first level wiring conductor is formed by means of electroplating using the conducting underlayer as an electrode to be plated, and the conductive pillar is formed by means of an electroplating using the conducting underlayer as the electrode to be plated.

5. A method claimed in Claim 4 wherein the conductive pillar is formed so that a top of the conductive pillar is lower than an upper surface level of the first photoresist layer.

6. A method claimed in Claim 5 further including the steps of removing the first and second photoresists, forming an insulating layer to cover the whole of the substrate but to allow a head portion of the conductive pillar to be exposed from the insulating layer.

7. A method claimed in Claim 6 further including the step of etching back the insulating layer so that the a head portion of the conductive pillar is protruded from the insulating layer.

8. A method claimed in Claim 7 further including the steps of forming a second conducting underlayer on the insulating layer, depositing a third photoresist layer on the second conducting underlayer and patterning the deposited third photoresist layer to form a second groove for formation of a second level wiring conductor in the deposited second photoresist layer, the second groove being positioned to cross the first level conductor in a plan view and to selectively pass on the first conductive pillars, forming a second level wiring conductor within the groove by means of electroplating using the second conducting underlayer as an electrode to be plated so that second level wiring conductor is selectively in electrical contact with the first conductive pillars, the second wiring conductor having a thickness smaller than that of the deposited second photoresist layer, forming a fourth photoresist to cover an area including the second wiring conductor, forming a second opening in the fourth photoresist above the second wiring conductor at a selected position so that a portion of the second wiring conductor is exposed through the second opening, the second opening having a size larger than a width of the second wiring conductor, and forming a second conductive pillar within the opening by means of an electroplating using the second conducting underlayer as an electrode to be plated, so that the second conductive pillar is formed in the second groove above the second wiring conductor, and removing